IN THE CLAIMS

1-50 (canceled)

51. (new) A network switch, comprising:

an input layer including N input layer circuits, each input layer circuit including an input layer circuit input port and N queues corresponding to N output terminals;

an intermediate layer including N intermediate layer circuits, each intermediate layer circuit including N buffers positioned between N intermediate layer circuit input terminals and N intermediate layer circuit output terminals; and

an output layer including N output layer circuits, each output layer circuit having N output layer circuit input terminals and an output layer circuit output port, said N output layer circuit input terminals corresponding to individual intermediate layer circuit output terminals of said N intermediate layer circuits;

wherein said output layer includes an output layer circuit configured to generate a back-pressure signal representative of the status of said output layer circuit; and

wherein said input layer includes an input layer circuit configured to be responsive to said back-pressure signal by selectively inserting flow control information into a data cell.

52. (new) A network switch, comprising:

an input layer to receive a data stream including a set of cells, each cell including data and a header to designate a destination device, said input layer including a set of input layer circuits, a selected input layer circuit of said set of input layer circuits receiving said data stream, said selected input layer circuit including a set of queues corresponding to a set of destination devices, said selected input layer circuit being configured to assign a selected cell from said data stream to a selected queue of said set of queues, said selected queue corresponding to a selected destination device specified by said header of said selected cell;

an intermediate layer including a set of intermediate layer circuits, each intermediate layer circuit including a set of buffers corresponding to said set of destination devices, a selected intermediate layer circuit of said set of intermediate layer circuits receiving said selected cell and

assigning said selected cell to a selected buffer corresponding to said selected destination device; and

an output layer including a set of output layer circuits corresponding to said set of destination devices, a selected output layer circuit of said set of output layer circuits storing said selected cell prior to routing said selected cell to a selected output layer circuit output node;

wherein said selected output layer circuit includes circuitry to produce a flow control warning signal in response to output layer congestion, said flow control warning signal being applied to said input layer, which produces a flow halt signal within a cell header, said intermediate layer including circuitry to identify said flow halt signal and alter the delivery of cells to said output layer.

53. (new) A network switch, comprising:

an input layer to receive a data stream including a set of cells, each cell including data and a header to designate a destination device, said input layer including a set of input layer circuits, a selected input layer circuit of said set of input layer circuits receiving said data stream, said selected input layer circuit including a set of queues corresponding to a set of destination devices, said selected input layer circuit being configured to assign a selected cell from said data stream to a selected queue of said set of queues, said selected queue corresponding to a selected destination device specified by said header of said selected cell;

an intermediate layer including a set of intermediate layer circuits, each intermediate layer circuit including a set of buffers corresponding to said set of destination devices, a selected intermediate layer circuit of said set of intermediate layer circuits receiving said selected cell and assigning said selected cell to a selected buffer corresponding to said selected destination device; and

an output layer including a set of output layer circuits corresponding to said set of destination devices, a selected output layer circuit of said set of output layer circuits storing said selected cell prior to routing said selected cell to a selected output layer circuit output node;

wherein said input layer, said intermediate layer, and said output layer are formed on a single semiconductor substrate, said network switch being configurable to enable a first region of said single semiconductor substrate selected from said input layer, said intermediate layer and

said output layer, while disabling two regions of said single semiconductor substrate selected from said input layer, said intermediate layer and said output layer.

54. (new) A network switch, comprising:

an input layer including N input layer circuits, each input layer circuit including an input layer circuit input port and N queues corresponding to N output terminals;

an intermediate layer including N intermediate layer circuits, each intermediate layer circuit including N buffers positioned between N intermediate layer circuit input terminals and N intermediate layer circuit output terminals; and

an output layer including N output layer circuits, each output layer circuit having N output layer circuit input terminals and an output layer circuit output port, said N output layer circuit input terminals corresponding to individual intermediate layer circuit output terminals of said N intermediate layer circuits;

wherein said input layer, said intermediate layer, and said output layer are formed on a single semiconductor substrate, said network switch being configurable to enable a first region of said single semiconductor substrate selected from said input layer, said intermediate layer and said output layer, while disabling two regions of said single semiconductor substrate selected from said input layer, said intermediate layer and said output layer.

55. (new) The network switch of claim 54, wherein each input layer circuit includes: a sorting circuit to route incoming cells to one of N destinations, each destination of said N destinations having a corresponding queue within said input layer circuit; and a transposer circuit coupled to said N queues and said N output terminals, said transposer circuit being configured to transpose cells stored in said N queues for delivery to said N output terminals.

56. (new) The network switch of claim 54, wherein each intermediate layer circuit includes: a sorting circuit to route incoming cells to said N buffers, said N buffers thereafter delivering said incoming cells to said N intermediate layer circuit output terminals.

57. (new) The network switch of claim 54, wherein each output layer circuit includes: a transposer circuit coupled to said N output layer circuit input terminals, said transposer circuit

being configured to transpose data cells received at said N output layer circuit input terminals; and an output layer circuit queue coupled to said transposer circuit and said output layer circuit output port.